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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,928	01/15/2004	Joseph Huang	ALTR:023	6328

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EXAMINER	
WEINBERG, MICHAEL J	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,928	HUANG ET AL.	
	Examiner	Art Unit	
	Michael J. Weinberg	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☒ Claim(s) *6-8 and 23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2/14/2005 was filed after the mailing date of the application on 1/15/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The disclosure is objected to because of the following informalities: In paragraph 38, "programmable interconnect circuitry 112" should most likely be 121.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Drawings

4. The drawings are objected to because they are informal. However, the drawings are suitable for examination.

5. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 6-8 and 23-26 are objected to because of the following informalities:

With regard to **claims 6-8**, "the plurality of circuit blocks" and "the programmable circuit elements" both have no antecedent basis in claim 3.

With regard to **claims 23-26**, "the coding of the coded signals" as no antecedent basis in claim 22.

All claims will be treated to the best of the examiner's ability. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6, 9-24, 27-30, 33, and 39-52 rejected under 35 U.S.C. 102(b) as being anticipated by Fuchigami et al (US patent 6,219,286).

With regard to **claim 1**, Fuchigami discloses an integrated circuit (figure 1) including redundancy circuitry 3 configured to provide redundancy by using a decoder circuitry 31, wherein the decoder circuitry 31 is configured to decode coded defect information received from a set of circuit elements 4 adapted to provide the coded defect information (abstract).

With regard to **claim 2**, Fuchigami discloses an integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy by bypassing a defective circuit block within the integrated circuit. (abstract- "so as to select, for the output signal line of the row decoder 2, one of the word lines except the defective word line in accordance with the arrangement order.")

With regard to **claim 3**, Fuchigami discloses an integrated circuit (IC) according to claim 2, wherein the redundancy circuitry is further configured to provide redundancy by using a redundant circuit block (memory cells on WL_{n+1} where n is the row number of the row with a defect) to perform the functionality of the bypassed defective circuit block (column 7, lines 1-7 and column 1, lines 57-61).

With regard to **claim 4**, Fuchigami discloses an integrated circuit (IC) according to claim 1, wherein the redundancy circuitry is further configured to provide redundancy for a plurality of circuit blocks (memory cells on WL_n) within the integrated circuit (IC).

With regard to **claim 5**, Fuchigami discloses an integrated circuit (IC) according to claim 3, wherein the set of circuit elements 4 comprise a plurality of programmable circuit elements (column 3, lines 25-30).

With regard to **claim 6,** as far as understood, Fuchigami discloses an integrated circuit (IC) according to claim 3, wherein a number of the programmable circuit elements (6 in figure 12) is smaller than the number of the circuit blocks (at least 9 rows in figure 1) in a plurality of circuit blocks.

With regard to **claim 9**, Fuchigami discloses an integrated circuit **(see figure 1, annotated below for at least claims 9-29)**, comprising:

means 4 for providing coded signals that correspond to a defect in a defective circuitry within the integrated circuit (abstract);

means 31 for decoding the coded signals to generate decoded defect signals (abstract); and

means (32 and 33) for providing redundancy in the integrated circuit in response to the decoded defect signals (abstract).

With regard to **claim 10**, Fuchigami discloses an integrated circuit (see figure 12) according to claim 9, wherein the number of decoded defect signals (totaling 12) is larger than the number of coded signals (totaling 6).

With regard to **claim 11**, Fuchigami discloses an integrated circuit (IC) according to claim 10, wherein, in response to the decoded defect signals, the means (32 and 33) for providing redundancy in the integrated circuit causes a redundant circuitry to be used instead of the defective circuitry (abstract, last 4 lines).

With regard to **claim 12**, Fuchigami discloses an integrated circuit (IC) according to claim 11, wherein the means 4 for providing the coded signals couples to the means 31 for decoding the coded signals via a first signal link.

With regard to **claim 13**, Fuchigami discloses an integrated circuit (IC) according to claim 12, wherein the means 31 for decoding the coded signals couples to the means for providing redundancy (32 and 33) via a second signal link.

With regard to **claim 14**, Fuchigami discloses an integrated circuit (IC) according to claim 13, wherein the defective circuitry WL_n comprises a memory circuit MC (column 18, lines 35-40).

With regard to **claim 15**, Fuchigami discloses an integrated circuit (IC) according to claim 14, wherein the redundant circuitry WL_{n+1} comprises a memory circuit MC (column 18, lines 35-40).

With regard to **claim 16**, Fuchigami discloses an integrated circuit (IC) according to claim 15, wherein the means (32 and 33) for providing redundancy couples to the defective circuitry WL_n via a third signal link.

With regard to **claim 17**, Fuchigami discloses an integrated circuit (IC) according to claim 16, wherein the means (32 and 33) for providing redundancy couples to the redundant circuitry WL_{n+1} via a fourth signal link.

With regard to **claim 18**, Fuchigami discloses a programmable logic device (which according to the specification of the applicant may include memory), comprising:

a plurality of programmable elements 4, the plurality of programmable elements configured to provide a first set of signals (through 1st signal link as illustrated);

a decoder circuit 31 coupled to the plurality of programmable elements 4, the decoder circuit configured to derive a second set of signals (through 2nd signal link as illustrated) from the first set of signals; and

redundancy circuitry (32 and 33) coupled to the decoder circuit, wherein the redundancy circuitry is responsive to the second set of signals (abstract).

With regard to **claim 19**, Fuchigami discloses a programmable logic device (PLD) according to claim 18, wherein the first set of signals comprises a set of signals configured to identify a defective circuit in the programmable logic device (abstract).

With regard to **claim 20**, Fuchigami discloses a programmable logic device (PLD) according to claim 19, wherein the set of signals (from register 4) configured to identify the defective circuit comprises coded signals (abstract).

With regard to **claim 21**, Fuchigami discloses a programmable logic device (PLD) according to claim 20, further comprising a redundant circuit (WL_{n+1} where n is the row number of the row with a defect), wherein, in response to the second set of signals (through 2nd signal link, the redundancy circuitry causes an input signal to be coupled to the redundant circuit instead of the defective circuit.

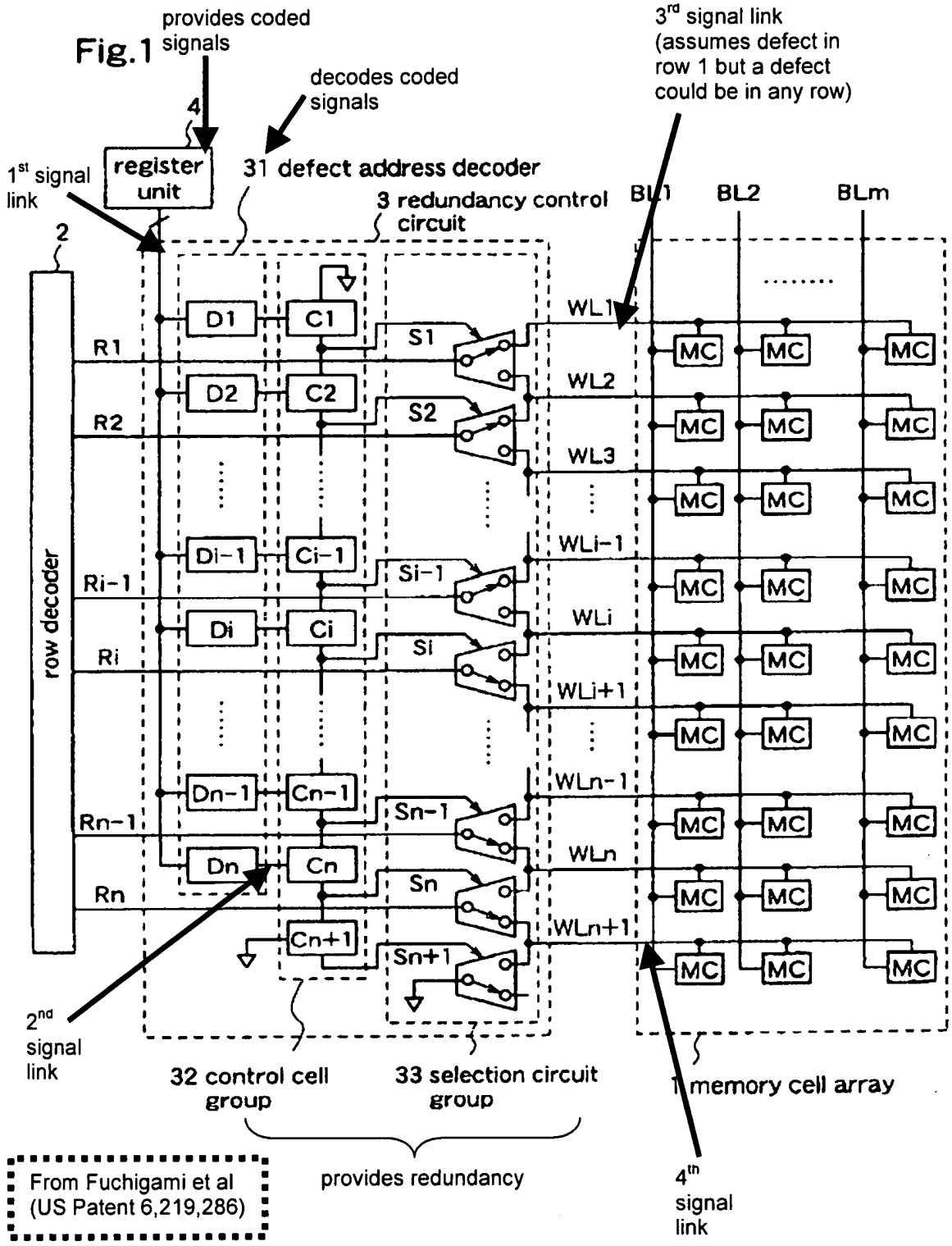
With regard to **claim 22**, Fuchigami discloses a programmable logic device (PLD) according to claim 21, wherein, in response to the second set of signals, the redundancy circuitry (32 and 33) causes an output signal of the redundant circuit to be used instead of an output signal of the defective circuit (abstract, last 4 lines).

With regard to **claim 23,** as far as understood, Fuchigami discloses a programmable logic device (PLD) according to claim 22, wherein a coding of the coded signals corresponds to information programmed in the programmable elements 4.

With regard to **claim 24**, Fuchigami discloses a programmable logic device (PLD) according to claim 23, wherein each of the programmable elements comprises a fuse (column 3, lines 35-30).

With regard to **claim 27**, Fuchigami discloses a programmable logic device (PLD) according to claim 22, wherein the defective circuit WL_n comprises a memory circuit MC, and wherein the redundant circuit WL_{n+1} comprises a memory circuit MC.

Fig.1


provides coded signals
4
register unit
decodes coded signals
31 defect address decoder
1st signal link
2
3 redundancy control circuit
3rd signal link (assumes defect in row 1 but a defect could be in any row)
BL1
BL2
BLm
row decoder
R1
R2
Ri-1
Ri
Rn-1
Rn
D1
C1
S1
D2
C2
S2
Di-1
Ci-1
Si-1
Di
Ci
Si
Dn-1
Cn-1
Sn-1
Dn
Cn
Sn
Cn+1
Sn+1
WL1
WL2
WL3
WLi-1
WLi
WLi+1
WLn-1
WLn
WLn+1
MC
2nd signal link
32 control cell group
33 selection circuit group
1 memory cell array
provides redundancy
4th signal link
From Fuchigami et al (US Patent 6,219,286)

With regard to **claim 28**, Fuchigami discloses a programmable logic device (PLD) according to claim 22, wherein the defective circuit comprises programmable logic circuitry MC, and wherein the redundant circuit (WL_{n+1} where n is the row number of the row with a defect) comprises programmable logic circuitry MC.

With regard to **claim 29**, Fuchigami discloses a programmable logic device (PLD) according to claim 22, wherein the defective circuit WL_n comprises programmable interconnect circuitry 33, and wherein the redundant circuit (WL_{n+1} where n is the row number of the row with a defect) comprises programmable interconnect circuitry 33.

With regard to **claim 30**, Fuchigami discloses a programmable logic device (PLD), comprising:

a first block of memory WL_n;

a plurality of programmable fuses 4, the plurality of programmable fuses configured to provide a set of coded signals corresponding to a defect in the first block of memory (abstract);

a decoder circuit 31 configured to derive a decoded set of signals from the coded set of signals (abstract);

redundancy circuitry (32 and 33) coupled to the decoder circuit, the redundancy circuitry configured to respond to the decoded set of signals; and

a second block of memory (WL_{n+1} where n is the row number of the row with a defect) coupled to the redundancy circuitry (32 and 33), wherein the second block of memory is used to provide redundancy for the first block of memory (column 7, lines 1-7 and column 1, lines 57-61).

With regard to **claim 33**, Fuchigami discloses a programmable logic device (PLD) according to claim 30, wherein the decoder comprises:

at least one inverter 121a-f adapted to receive the coded signals; and

at least one AND gate (122a-f, 123a-f, 124a-f) coupled to the at least one inverter, wherein the at least one AND gate provides the decoded set of signals.

With regard to **claim 39**, Fuchigami discloses a programmable logic device (PLD) according to claim 30, further comprising programmable logic circuitry MC coupled to the second memory block.

With regard to **claim 40**, Fuchigami discloses a programmable logic device (PLD) according to claim 30, further comprising programmable interconnect circuitry 33 coupled to the second memory block.

With regard to **claim 41**, Fuchigami discloses a method of providing redundancy in an integrated circuit (IC), the method comprising:

retrieving information (from register unit 4) about a defect in the integrated circuit (IC), wherein the information about the defect is coded in the integrated circuit (abstract);

decoding (using decoder 31) the information about the defect to identify a defective circuit within the integrated circuit (abstract); and

using a redundant circuit (WL_{n+1} where n is the row number of the row with a defect) within the integrated circuit (IC) instead of the identified defective circuit WL_n (column 7, lines 1-7 and column 1, lines 57-61).

With regard to **claim 42**, Fuchigami discloses a method according to claim 41, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information coded in a set of programmable elements 4 within the integrated circuit (abstract).

With regard to **claim 43**, Fuchigami discloses a method according to claim 42, wherein decoding the information about the defect to identify a defective circuit within the integrated circuit (IC) further comprises generating a set of decoded signals (using decoder 31) from the information about the defect (abstract).

With regard to **claim 44**, Fuchigami discloses a method according to claim 43 (see figure 12), wherein the number of signals in the set of decoded signals (totaling 12) is larger than the number of programmable elements in the set of programmable elements (totaling 6).

With regard to **claim 45**, Fuchigami discloses a method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises bypassing the identified defective circuit (abstract).

With regard to **claim 46**, Fuchigami discloses a method according to claim 43, wherein using a redundant circuit within the integrated circuit (IC) instead of the identified defective circuit further comprises routing (thanks to selection circuit group 33) a set of input/output signals (through R_n) to the redundant circuit instead of the identified defective circuit (abstract).

With regard to **claim 47**, Fuchigami discloses a method according to claim 46, wherein routing (thanks to selection circuit group 33) a set of input/output signals to the redundant circuit instead of the identified defective circuit further comprises:

routing an input signal to the redundant circuit instead of the identified defective circuit; and

using an output signal of the redundant circuit instead of an output signal of the identified defective circuit (all in abstract).

With regard to **claim 48**, Fuchigami discloses a method according to claim 43, wherein retrieving information about a defect in the integrated circuit (IC) further comprises retrieving information that is generated by testing the integrated circuit (IC) to identify a defective circuit (inherent), and coding the information about the defect in the set of programmable elements (column 6, lines 12-13).

With regard to **claim 49**, Fuchigami discloses a method according to claim 48, wherein the integrated circuit (IC) comprises a programmable logic device. (As in the title, a memory is used which according to the specification of the applicant is used in a PLD.)

With regard to **claim 50**, Fuchigami discloses a method according to claim 49, wherein the defective circuit WL_n comprises a memory circuit MC within the programmable logic device (PLD).

With regard to **claim 51**, Fuchigami discloses a method according to claim 50, wherein the defective circuit WL_{n+1} comprises programmable logic circuitry MC within the programmable logic device (PLD).

With regard to **claim 52**, Fuchigami discloses a method according to claim 50, wherein the defective circuit WL_{n+1} comprises programmable interconnect circuitry 33 within the programmable logic device (PLD).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7, 8, 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchigami in view of Yamada (US Patent 4,747,080).

With regard to **claims 7, 8, 25, 26, 31, and 32**, Fuchigami discloses an integrated circuit (IC) according to claim 6 and programmable logic devices (PLD) according to claims 24 and 30, as far as understood, but does not teach a particular type of fuse in use such as laser programmed or electrically programmed fuses.

However, Yamada does teach a device with redundancy wherein each of the programmable circuit elements (for storing an address of a defect) comprises an electrically programmed fuse or laser-programmed fuse (column 13, lines 50-65), as is common in the art.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a laser-programmed or electrically programmed fuse in the invention of Fuchigami in order to cheaply store the address of a defect.

11. Claim 34-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchigami in view of the Application Prior Art C6 "MRAM redundancy Scheme" (which will be further referred to as C6).

With regard to **claims 34-38**, Fuchigami teaches the device of claim 30, but does not show the limitations of claims 34-38. However, C6 does teach a redundancy circuitry comprising a set of flip-flops configured to receive a decoded set of signals D[n] from a decoder circuit.

With regard to **claim 35**, C6 teaches that the redundancy circuitry further comprises a set of OR gates, wherein each OR gate in the set of OR gates couples to a respective flip-flop in the set of flip-flops.

With regard to **claim 36**, C6 further teaches that the redundancy circuitry further comprises a set of multiplexers, wherein each multiplexer in the set of multiplexers couples to a respective OR gate in the set of OR gates.

With regard to **claim 37**, C6 further teaches a first multiplexer in the set of multiplexers couples to the first block of memory.

With regard to **claim 38**, C6 further teaches a second multiplexer in the set of multiplexers that couples to the second block of memory.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the device of Fuchigami with the redundancy circuit of C6 in order to allow a switching away from defective cells to spare cells.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Agrawal (US Patent 6,366,508) discloses redundancy device with stored coded information about a defective memory cell.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Weinberg whose telephone number is 571-272-6424. The examiner can normally be reached on M-F 9:00 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mjw